USN 10CS74

Seventh Semester B.E. Degree Examination, July/August 2022
Advanced Computer Architectures

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain how computer Architect must design a computer to meet functional requirement and cost of an IC of a system. **(10 Marks)**

b. Suppose we have made the following measurements :
Frequency of FP operations = 20%
Average CPI of FP operations = 5.0
Average CPI of other instructions = 2.0
Frequency of FPSQR = 3%
CPI of FPSQR = 15
Assume that the 2 design alternatives are to decrease the CPI of FPSQR to 2 or 10 decrease the average CPI of all FP operations to 2.5. Compare these two design alternatives using the processor performance equation. **(06 Marks)**

c. What is dependability? Explain 2 main measures of dependability. **(04 Marks)**

2 a. Explain how pipelining is implemented of every MIPS instruction at most considering five clock cycles. **(10 Marks)**

b. What are the major hurdle of pipelining? Illustrate the structural Hazards in detail. **(10 Marks)**

3 a. Show how the loop would look on MIPS, for the following code segment including any stalls or idle clock cycles.
i) Scheduled and unscheduled loop
ii) Merging and unrolled loop. **(12 Marks)**

b. Explain control dependence of the following code segment

```
if P1 {
      S1;
   };
if P2 {
      S2;
   }
```

(08 Marks)

4 a. What are the steps involved in handling an instruction with a branch target buffer? **(08 Marks)**

b. Explain an Analysis of the performance Pentium 4 with respect to branch prediction and cache misess SPEC CPU 2000 benchmarks. **(08 Marks)**

c. What are the general issues involved in implementation of speculations? **(04 Marks)**

PART – B

5 a. With a neat diagram, explain directory Based cache coherence protocol state transition diagram. (12 Marks)

b. Explain the general models of memory consistency with a 2 code segments. (08 Marks)

6 a. With respect to virtual memory differentiate the following :

i) Caches Vs virtual memory

ii) Paging Vs segmentation (12 Marks)

b. Suppose that in 1000 memory references there are 40 misses in the I^{st} level cache and 20 misses in II^{nd} level caches. What are the various miss rates? Assume miss penalty from L2 to memory is 200CC, the hit time of L2 cache is 10CC, then hit time of L1 is 1CC and there are 1.5 memory reference per instruction. What is the average memory access time and average stall cycles per instruction? Ignore the impact of writes. (08 Marks)

7 a. Explain Nineth optimization of cache performance to reduce miss rate of complier. (12 Marks)

b. Explain the impact of virtual machines on virtual memory and I/O. (08 Marks)

8 a. Explain loop level parallelism for the Greatest Common Divisor (GCD) test and identify the drawback of dependence analysis. (12 Marks)

b. Define Predicated Instruction, what are the limitations of Predicated instructions. (08 Marks)

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